EXTC /VI /CBC

10/6/2019

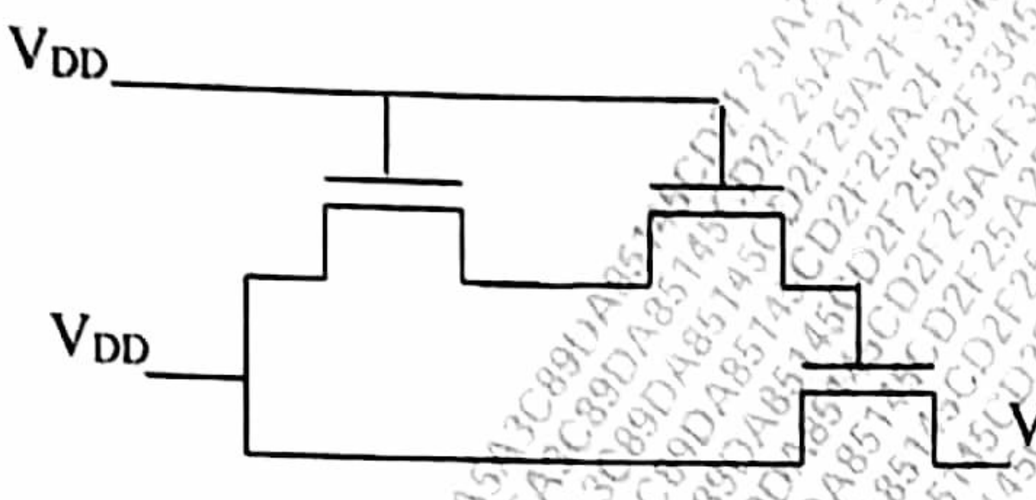
Paper / Subject Code: 37006 / VLSI DESIGN

Time: 3 Hours **Marks: 80**

] Question no.1 is **compulsory**
] Attempt any **three** questions out of remaining questions
] Assume **suitable data** if **required**
] **Figures** to the **right** indicate marks.

. No. 1) Solve the following [20]

a) Calculate the voltage at the output node V_o if V_{DD}=5V and V_{th}=1.5V



b) Draw and Explain Clocked SR latch using static CMOS design style.
c) Draw layout diagram of static CMOS inverter based on lambda design rules.
d) Draw VTC of static CMOS inverter and show operating regions of nMOS and pMOS transistors on it.
e) Explain short channel effects (any two).

. No. 2)

a) Explain in detail the fabrication process steps for a CMOS inverter using n- well process with the help of cross sectional view for each step. [10]

b) Implement a two input XOR gate using
(i) static CMOS logic
(ii) Dynamic logic
(iii) Transmission gate
(iv) Pseudo NMOS logic [10]

. No. 3)

a) Derive an expression for the inverter threshold voltage (switching voltage) of a CMOS inverter. Calculate the (W/L) ratios of the NMOS and PMOS transistor in the CMOS inverter circuit with the following parameters:
V_{DD} = 3V $V_{t0,n}$= 0.6V $V_{t0,p}$ = -0.8V V_{TH}=1.5V
$\mu_n C_{OX}$=60μA/V² $\mu_P C_{OX}$ =20μA/V² [10]

b) Draw schematic diagram of six transistor SRAM cell and explain its Read and Write operations. [10]

Q. No. 4)

a) What is scaling. Compare constant field scaling with constant voltag state advantages and limitations in both the methods.

b) Design a 4- bit CLA adder using dynamic NMOS logic. Compare circuit with respect to a 4 bit ripple carry adder.

Q. No. 5)

a) Draw the CMOS circuit for $Y = \overline{A + BC(D + E) + F}$ and find CMOS inverter circuit for simultaneous switching of all inputs, $(W/L) = 15$ for all pMOS transistors and $(W/L) = 10$ for all nMOS tr

b) Explain in detail static and dynamic power dissipation. What are the components which make power dissipation in CMOS circuit?

Q. No.6) Explain any 2 of the following

a. 4 bit Array Multiplier
b. Interconnect Delay model
c. 3-T DRAM